IN THE SPECIFICATION:

Delete the paragraph beginning at page 7, line 8 and replace it with the following new paragraph:

FIG. 3 shows the format of the disk 40 appearing in FIG. 2 and the format of each ~~serve~~ servo area 410 provided in the disk 40;

Delete the paragraph beginning at page 16, line 27 and replace it with the following new paragraph:

The MUX 13 selects the write gate signal WG1a output from the read/write controller 11, and outputs it as the write gate signal WG1 through the terminal 101. At this time, the switch SW1 is in the OFF state. Accordingly, the write gate signal WG1a is prevented from being input to the write inhibition controller 12. Thus, in the first mode, the write gate signal WG1a is prevented from being used for data write inhibition control. The write gate signal WG1 (= WG1a) output from the terminal 101 of the HDC 10 is supplied to the ENDEC 21 in the read/write channel 20 connected to the HDC 10. As mentioned above, the read/write channel 20 is supplied with the one-sector write data, shown in FIG. 4G, output from the read/ write controller 11 in units of bytes. The ENDEC 21 receives this write data in accordance with the write gate signal WG1 (= WG1a), and encodes it. At this time, based on the write gate signal WG1 (= WG1a) shown in FIG 4C or 4F, the ENDEC 21 generates the write gate signal WG2 shown in FIG. 4D or 4I, which reflects a delay in a data output caused by the encoding process in the ENDEC 21. The period in which the write gate signal WG2 is asserted is made longer, by the encoding delay time T2, than the period in which the write gate signal WG1 (= WG1a) is asserted. In other words, the period in which the write gate signal WG2 is asserted is made longer by the period T2 ranging from the time point t2 at which the write gate signal WG~~+~~1 (= WG2a) is negated, to a time point t4 at which encoding of the one-sector write data completely finishes (T2 = t4 - t2).

Delete the paragraph beginning at page 19, line 15 and replace it with the following new paragraph:

To avoid this, the write inhibition controller 12 monitors the servo identification signal SI and the write gate signal WG2 from the read/write channel 20 in the first mode, thereby detecting whether the write inhibition requirement is satisfied. Specifically, if the period in which the servo identification signal SI is asserted overlaps the period in which the write gate signal WG2 is asserted, the write inhibition controller 12 regards this overlapping period as the period in which the write inhibition requirement is satisfied (i.e., the HDD is in the write inhibition state). In the examples of FIGS. 4A and 4D, only during the period T3 from a time point t5 to a time point t6, both the servo identification signal SI and write gate signal WG2 are asserted. Therefore, the write inhibition controller 12 detects that the period T3 is the period in which the HDD is in the write inhibition state, thereby inhibiting the write gate signal WG2 from passing through the controller 12 during the period T3, with the level of the signal unchanged. In other words, in the first mode, the write inhibition controller 12 permits the write gate signal WG2 to pass therethrough and be output as the write gate signal WG2' through the output port 124 as shown in FIG. 4E, only when the servo identification signal SI is negated. As is apparent, the write gate signal WG2' is negated regardless of the state of the write gate signal WG2, when the servo identification signal SI is ~~negated~~ asserted.

Delete the paragraph beginning at page 21 line 7 and replace it with the following new paragraph:

When the write inhibition state is not detected, the head IC 30 causes the head 50 to write, into a target sector on the disk 40, the encoded write data, shown in FIG. 4H, output from the read/write channel 20 in accordance with the write gate signal WG2'. As a result, data writing considering the encoding delay time in the read/write channel 20 can be realized. On the other hand, when the write inhibition state is detected, the write gate signal WG2' reflects the write inhibition state. In other words, the write gate signal WG2' is forcibly negated during the period in which the write inhibition state is detected. Accordingly, during the period in which the write inhibition state is detected, the head IC 30 inhibits the head 50 from writing data to the disk 40. As a result, the servo data written in the ~~serve~~ servo area 410 is protected from breakage.